International Conference on Control, Engineering & Information Technology (CEIT'13)
Proceedings Engineering & Technology - Vol.1, pp.198-201, 2013

Multi-Islands Single-Electron Devices

Amine Touati[#1], Samir Chatbouri[*2], Adel Kalboussi[#3]

[#]*Physics Department, Faculty of Science of Monastir*
Tunisia
[1]Amine.Touati@istls.rnu.tn
[3]Adel.Kalboussi@fsm.rnu.tn

[*] *Physics Department, Faculty of Science of Monastir*
Tunisia
[2]Samir.chatbouri@yahoo.com

***Abstract*— The extremely high difficulty to process a Single-electron device with a unique single island connected between two tunnel junctions has motivated researchers to develop single electron devices with multiple islands. In this paper, we present a comparison of carriers transport through devices based on poly-metallic grains in one, two and three dimensional structure.**

***Keywords*—Single-electron devices (SED), Multi-Tunnel Junction (MTJs), two dimensional arrays (2D), three dimensional arrays (3D), Single-Electron Memory (SEM).**

I. INTRODUCTION

The ITRS [1] is for the last years considering many types of Single-Electron Device (SEDs) as possible post-CMOS devices in terms of speed, size, cost or power some applications. However, the range of applications for SED is very large, including sensors, actuators and optical application. The quantum effects (discreteness of energy levels) in ultrasmall islands, is the importance key in such devices. But Quantization effects could be problematic for the practical operation, if any dot traps an electron; it blocks other electrons flow due to Coulomb repulsion, and Coulomb blockade (CB) takes place. The technological difficulty is in fabricating SEDs such as Single Electron Transistors (SETs) [2] in the nanometer size range.

An alternative approach is the Multi-islands SETs, multi-island devices can be considered as multiple SETs connected to each other in series, or in parallel, one of the major advantages of multi-island devices comes from the fact that it requires a much simpler fabrication procedure than single-dot structures. Several multi-islands SETs based on poly-Si [220], metal [3], Si Quantum-Dots (QD) [4], or monocrystalline Si [5] have already been reported.

This work shows the advantage of MTJs in the context of a comparison of various SETs with MTJs structures and reports the specific electrical properties of these devices, operated from 4.2K to 300K, as candidates for new functionality of hybrid nano- memory applications circuit.

II. DEVICE STRUCTURE AND PARAMETERS

Single Electron Transistors (SETs) architecture in Figure.1 is quite similar to the MOSFET architecture, with a source, a drain, and a gate. The main difference is that, in the SET configuration, the channel is replaced by an ultra-small conductive island (capacitively coupled to the gate), with a gate capacitance C_G, and separated from Source-Drain by two tunnel barriers. The tunnel junctions are then electrically defined by a tunnel capacitance (C_T) and resistance (R_T) The operation of SET exploits the discrete number of charges in the conductive island.

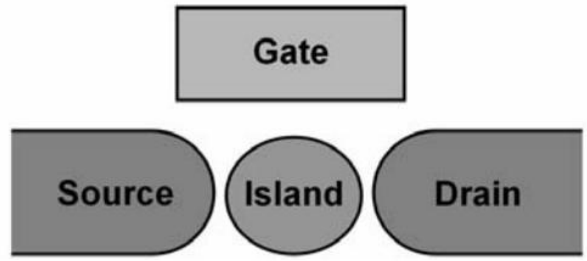

Figure.1. Basic structure of SET schematics

The equivalents circuits of the two dimensional (2D) of multi-islands SETs used for simulations is shown in Figure.2 For the simulations, the grains are electrically modeled as dots connected to their neighbors by tunnel junction, capacitances C_T, tunnel resistances R_T, and sharing a common gate. A gate is designated by a capacitance C_G, to each dot. Also a second gate can be added to the device.

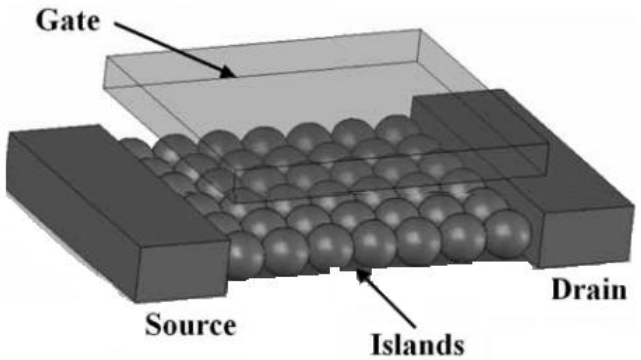

Figure.2. 7x6 regular multi-islands systems. Each island is controlled electrostatically by the gate, and is separated from its neighbour by a tunnel junction

The other type proposed of multi-islands SETs is the three dimensional (3D) structure. In this case we have

arranged the 2D structure in a vertical succession. In Figure.3 we have schematically a structure of three plans of 3x3 regular two dimensional MTJs. This system may have one or two or gates.

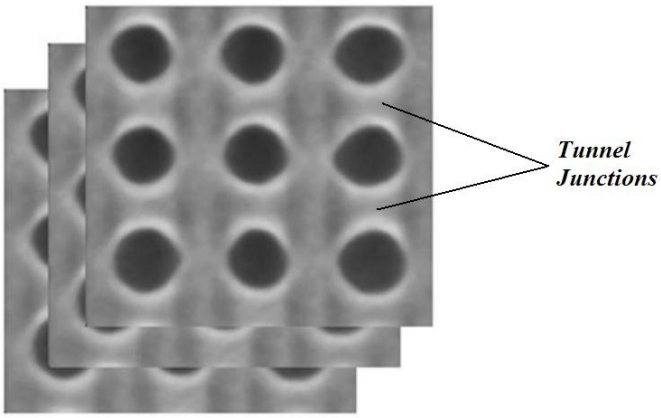

Figure.3. Three planes of 3x3 regular 2D multi-islands structures

III. Results and Discussions

A. *Monte Carlo Simulation of Structures Characterizations at low and high temperature*

The next results presented have shown that Monte Carlo (MC) simulations (using SIMON software [6]) appear to be an adequate tool for the prediction of electrical behavior of multiple-dot systems connected in arrays of tunnel junctions. However, grain sizes, gate and tunnel capacitances, tunnel resistances and dimensions have to be very well known or estimated. For the simulations in 2D, the dots are electrically modeled as dots connected to their neighbors by four tunnel junction with tunnel capacitances of 0.1aFand tunnel junction resistances of 1MΩ. The gate capacitance about 0.01aF and is connected to each dot. For the 3D the dots are connected to their neighbors by six tunnel junction, the tunnel capacitances and resistances are taken the same of the values of 2D. Consequently, each island can be considered as QDs and these QDs may behave as excellent traps for one or few electrons.

Figure 4 shows MC simulated drain current versus drain voltage ($I–V_{DS}$) characteristic for a simple SET, 2D (3×5 dot arrays) and 3D (3×3×5 dots arrays) devices at 300K. Despite the tunnel junction capacitances and gate capacitances in a single-dot SET are much lower than the intrinsic capacitance of a high temperature operation ($C_\Sigma << e^2/2k_BT$; where C_Σ is the island capacitance, e is the elementary charge, k_B is the Boltzmann constant and T is the temperature), the behavior of the SET loses its basic property: Coulomb staircase, and behaves like a simple diode. It is however to consider that only in SET with s we can observe the coulomb stairs but in either MTJs structure is clear that with symmetric and asymmetric structures also that this phenomenon

But on the other side, this phenomenon persists in the 2D and 3D dot arrays. Therefore analyzing the exactly theory of 2D and 3D array is a very complex task. Nevertheless, as shown on Figure.4 at room temperatures, each island as a single-dot of SET to offer extra Coulomb blockade region in $I–V_{DS}$ characteristics. We note that the total island capacitance in the 2D structure is becomes $4C_T + C_G$, and for the 3D structure is $5C_T + C_G$ for the upper and under planes and $6C_T$ for the planes between them due to the series and parallel combination of C_T.

At V_{DS} lower than ~1,2V, the multi-islands SETs is electrically blocked. For V_{DS} higher than 1,25V, the Fermi-level energy of electrons is decreased and the island energy level becomes transparent to them (conduction takes place by tunneling).

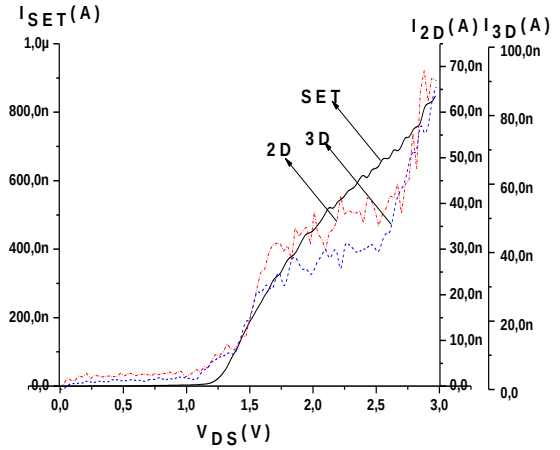

Figure.4. I-V_{DS} characteristics of a SET, 2D and 3D at 300K (C_G=0,01aF)

Figure 5 compares characteristic of two types of equivalent MTJs devices at different temperatures. This characteristic shows that low and high temperature has no remarkable effect on the functioning of the system, but we note that the background charges have more impact at high temperature. Therefore replace the single-island by multiple islands, multi-island being insensitive to random background charges.

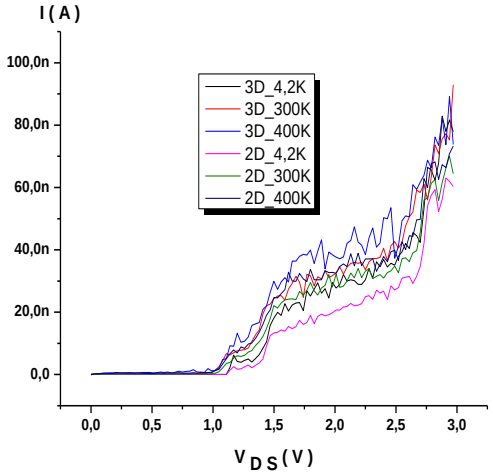

Figure.5. Temperature effect on the 2D and 3D structure

Figure.6 demonstrated at low and room temperature, that for such structure, the number of oscillations is maximal at 4,2K for 2D structure, and an extra valley of coulomb oscillation for the 3D device at range of temperatures (4,2K and 300K).

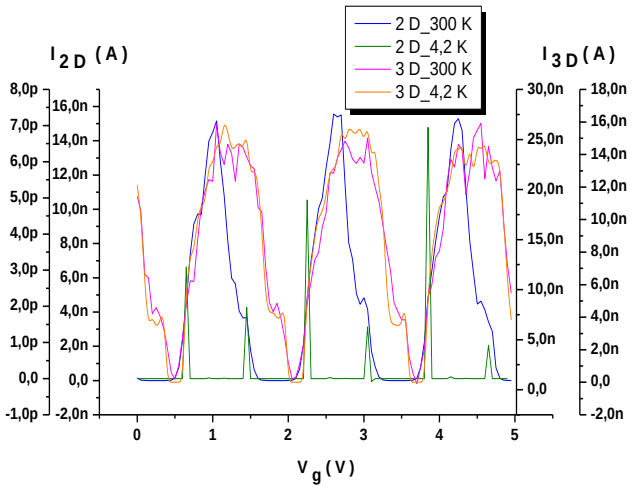

Figure.6. Monte Carlo simulation of Coulomb oscillation for 2D and 3D structures at low and high temperature and V_{DS}=0.5V

Therefore, as the gate voltage is increased at constant drain voltage, more electrons are flowing through the array and thus the gate current increases. The tunneling current increase with increasing temperature and oscillations are becoming much more clearly periodic. It is interesting to note that increasing the temperature could allow a recovery of oscillations periodicity similar to the SET.

As the temperature increases the thermal energy becomes lower than $e^2/(4C_T+C_G)$ in 2D case (lower than $e^2/(5C_T+C_G)$ in the 3D device) , this is shown in Figure.6 by a small widths of Coulomb Blockade zone in the 2D than the 3D devices.

Simulation of I-V_{GS} represented at 300K for four different drain voltages show that the coulomb oscillation should increase with an increase of the drain voltage in the 2D and 3D devices. This is verified on Figure.7 where the high regularity of resulting oscillations makes their exploitation easy for nanoelectronics integrated circuits applications.

CB has been shown at low temperature, and more effective COs has been observed at higher drain voltages. MC simulations performed prove the irregular oscillations in poly-islands systems make their exploitation for SET applications possible.

B. Title and Author Details Memory Application

We have shown that the MTJs-SET can be used as a current sensing device for very low current measurements with a resolution better than 1pA. Multi-islands devices may be are more suitable for memory applications because the size dispersion and position of the islands is less restricting [7]. In Figure.8 we schematize the memory cell, it consist of 2D MTJs arrays coupled with a single-electron box (SEB) [8,9]. The coupling is with an oxide modeled by a capacity C_C. "Set" and "Reset" states can be done within a single step from V_{GS} or V_{DS}.

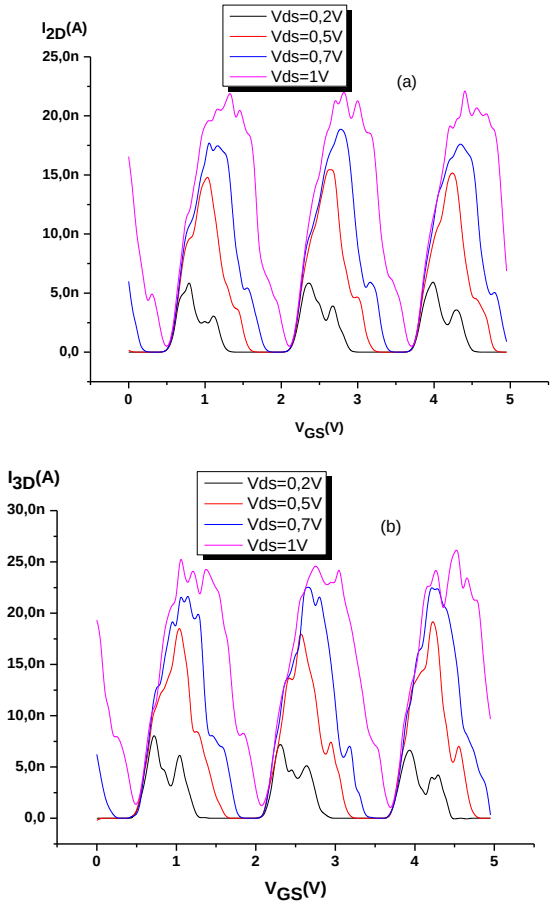

Figure.7. Gate current simulation at 300K for different drain voltages (a) I_{2D}-V_{GS} (b) I_{3D}-V_{GS}

Initially the memory cell stores the logical “0”, i.e. no excess electrons are present in the memory node. For writing “1”, a positive bias is first applied, which corresponds to 1 electron in the memory node. A negative voltage pulse is then applied for inject electron outside the memory node.

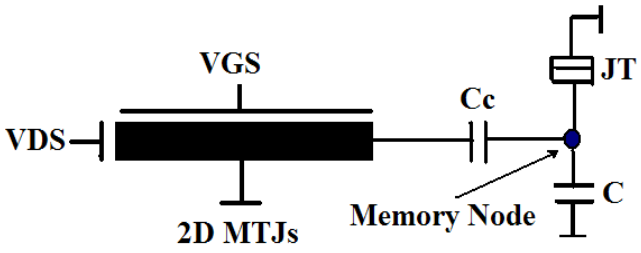

Figure.8. Memory cell proposed with 2D structure.

To add one electron to the memory dot requires a voltage increment of e/C_{2D} to be applied to the memory voltage, where C_{2D} is the total capacitance 2D-MTJs system.

Figure.9 shows the memory effect on the node memory (island of SEB) with four electrons at 300K. When the V_{DS}

take the value of 3V; 4 electrons are confined in the memory island,

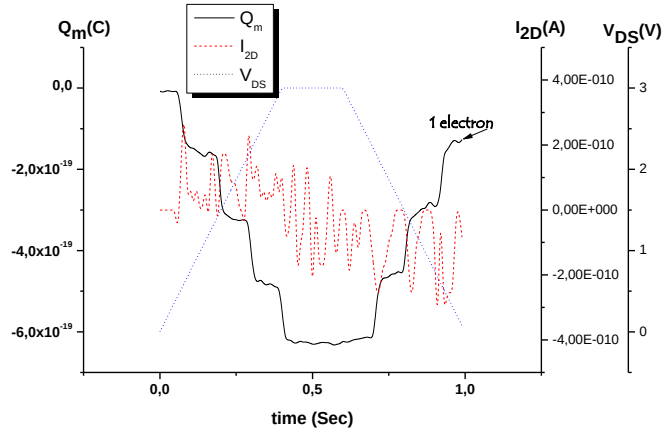

Figure.9. Simulation results of the logical "1" and "0" at 300K, the applied voltages in write/erase operation and 2D-MTJs current

and when the polarization is swept from 3V to 0V, 3 electrons are ejected from the QD memory and a hysteresis current appears in the electron accumulation regime of the MTJs-SET. This hysteresis can be explained by charge trapping in the MTJs islands. So the electrostatic and quantum confined phenomena are the most probable effects of this memory effect.

IV. Conclusions

We have shown that the Multi-island SET, in two dimensional and three dimensional, as a good candidate for a SET for room temperature operation. Coulomb blockade has [10] been shown at low temperature and observed at higher and lower drain voltages. Memory application is also demonstrate with 2D the electrostatic and quantum confined is the memory effect of stored bit

References

[1] International Technology Roadmap for Semiconductors (ITRS), 2009 Edition, Available online: http://public.itrs.net/

[2] D. V. Averin and K. K. Likharev, in "Mesoscopic Phenomena in Solids," B. L. Altshuler, P. A. Lee, and R. A. Webb, Eds. Elsevier, Amsterdam, 1991.

[3] W. Chen, and H. Ahmed, "Metal-based single electron transistors", Journal of Vacuum Science and Technology B, vol. 15 (4), pp. 1402-1405, 1997

[4] I. Kim, S. Han, H. Kim, J. Lee, B. Choi, S. Hwang,, D. Ahn, and H. Shin, "Room Temperature Single Electron Effects in Si Qantum Dot Memory with Oxide-Nitride Tunneling Dielectrics", Technical Digest of the International Electron Devices Meeting IEDM 1998, pp. 111-114, 1998.

[5] I. S. Jacobs and C. P. Bean, "Fine particles, thin films and exchange anisotropy," in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.

[6] C. Wasshuber, H. Kosina and S. Selberherr, "SIMON: a simulator for single-electron tunnel devices and circuits", IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, vol. 16 (9), pp.937-944, 1997.

[7] K. Uchida, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, "Silicon single-electron tunneling device fabricated in an undulated ultrathin silicon-on-insulator film", Journal of Applied Physics , vol. 90 (7), pp.3551-3557, 2001.

[8] Devoret M.H., Esteve D. and Urbina C, "Single-electron transfer in metallic nanostructures," Nature 360: 547–553 (1992).

[9] Lambe J. and Jaklevic R.C. "Charge-quantization studies using a tunnel capacitor," Phys Rev Lett 22: 1371–1375 (1969).